Influence of Chemical Cleaning Procedures and Thermal Oxidation Processes on the Uniformity of MOS Gate Oxides on Abrupt Steps on Silicon Surfaces

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***Abstract*—This work analyzes the influence of some chemical steps used in standard cleaning recipes on the surface micro-roughness of silicon wafers. The effect of varying the ammonium hydroxide concentration in the NH_4OH: H_2O_2:H_2O solution was studied and silicon wafer micro-roughness was characterized by atomic force microscopy technique at different scans of 1μmx1μm. Based on the results, it was possible to point the condition to obtain low surface micro-roughness for NH_4OH-based solutions with the lowest NH_4OH content before the growth of gate oxides. Following, it silicon-oxide thin films were grown onto periodic rectangular shapes, 100 nm in height, obtained by localized plasma etching on silicon wafer surfaces. Silicon oxides (SiO_2), about 4.5 nm thick, were grown in ultrapure dry-O_2 or pyrogenic (O_2 + H_2) environments in order to compare the planar uniformity and the grade of coverage at the step edges of rectangular shapes defined onto silicon surfaces. Pyrogenic and conventional oxidation at 850 ºC allowed one to obtain gate oxides on 100 nm-stepped silicon surfaces with high dielectric breakdown field (>10 MV/cm), good planar uniformity and conformal coverage at the step edges. The impact of this result is now the feasibility of fabricating good-quality gate oxides for surrounding gate transistors (SGT's) and texturized MOS solar cells.**

***Keywords*—Chemical Cleaning, MOS structure, silicon oxide growth.**

I. Introduction

The search for the increase of the device integration in integrated circuits is characterized by a marked reduction in the vertical and horizontal dimensions [1,2]. This reduction in the dimensions of the devices is accompanied by an improvement of their performance for surrounding gate transistors [2]. Also, the reduction of the gate oxide thickness has become an important technological issue related to MOS solar cells [3].

Literature reports that less rough Si/SiO_2 interfaces leads to lower leakage currents through the gate oxide layer, lower concentrations of traps at the $Si\text{-}SiO_2$ interface and higher dielectric breakdown fields [4-7]. Thus, in order to maintain or even increase the quality of the oxides, despite the reduction in thickness, greater care and greater control of the obtaining process is necessary. Parameters such as temperature, metallic contamination on the wafer surfaces or in the cleaning solutions, immersion speed of the wafers in the solutions and the hydrophilic or hydrophobic characteristic of the wafers, all affect the surface roughness before the gate oxidation [8]. A parameter to be highlighted is the amount of NH_4OH in the SC1 solution (Standard Cleaning 1). The smaller the amount of NH_4OH, the longer the time required for the removal of particles [8]. However, the $NH_4OH/H_2O_2/H_2O$ solution in the proportion of 0.2/1/5, after 10 minutes, shows the same efficiency in the removal of particles as in the proportion of 1/1/5 [9], while the reduction in the concentration of NH_4OH is followed by a reduction in the surface roughness of silicon wafers [8].

Another important fact to be highlighted is when reducing the thickness of the gate oxide of a device (capacitor or transistor) and the applied voltage is not reduced by the same scaling factor. In this case, there is an increase of the average electric field through the gate dielectrics, that is, it is submitted to a more critical condition of average electric field, requiring an improvement in the manufacturing quality of the same [1,10]. In addition, as already mentioned, as the thickness of the gate dielectric material is reduced, factors such as roughness and, also, organic and metallic contaminants become even more harmful when one wants to obtain a good manufacturing quality (low effective electric charge density and high dielectric breakdown field) [10-17]. Conventional and pyrogenic dry oxidation processes have been used to obtain SiO_2 with a thickness around 4 nm for manufacturing MOS gates. The conventional dry oxidation process can be described by the following reaction [18,19]:

$$Si + O_2 \rightarrow SiO_2 \quad (1)$$

For pyrogenic oxidation, initially hydrogen reacts with oxygen generating water molecules followed by their reaction with the silicon surface as follows [18,19]:

$$2H_2 + O_2 \rightarrow H_2O \quad (2)$$

and

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad (3)$$

The aim of this article is to analyze the influence of the chemical cleaning procedure and the oxidation recipe (conventional or pyrogenic) on the manufacturing quality and uniformity of silicon oxides on irregular Si surfaces containing abrupt steps.

II. Experimental Procedures

First, it was analyzed the solution that constitutes the first part of the known RCA cleaning [10] which in turn is known as standard cleaning number 1 (SC1 - Standard Cleaning 1). Below, the description of four variations of the SC1 with four concentrations of NH_4OH and two temperatures (71ºC and 84ºC) are presented.

Bath 1: $4H_2O$:H_2O_2 (30%):0,25NH_4OH(35%) 71º e 84ºC
Bath 2: $4H_2O$:H_2O_2 (30%):1NH_4OH (35%) 71º e 84ºC
Bath 3: $4H_2O$:H_2O_2 (30%):2NH_4OH (35%) 71º e 84ºC
Bath 4: $4H_2O$:H_2O_2 (30%):5NH_4OH (35%) 71º e 84ºC

For all tests, 3-inch p-type wafers were used, doped with boron, orientation <100>, resistivity in the range of 1 to 10Ωcm and thickness of 381±5μm. These wafers were cleaved into four equal parts and each of these parts was assigned to each of the solutions described. The different solutions were heated to reach different temperatures (71º and 84ºC) and the pieces of wafers were individually immersed for 15 min. in these solutions. To obtain better temperature control and minimize a possible imbalance caused by preferential evaporation of a certain component (H_2O_2 or NH_4OH), a glass lid was used over the beaker with a hole through which a thermometer was placed to control the temperature. After immersion in the different solutions, the samples were rinsed in DI water for 5 min., followed by drying in a ultrapure nitrogen jet. The time interval between the end of the sample preparation and the atomic force microscope (AFM) analysis was approximately 12 hours. During this time interval, the samples were placed in a properly cleaned glass sample box, which in turn were kept in a clean room environment until the AFM analysis. Then, using AFM, the surface roughness values were obtained. For the atomic force microscopy analysis, the equipment "Atomic Force Microscopy – Nanoscope E Digital, Inc." was used.

In the moment that preceded the AFM measurement, the samples were then cleaved into pieces of approximately 1 cm x 1cm to be positioned on the sample holder of the Nanoscope. Then 1 μm x 1μm scans were measured using a standard silicon nitride tip, also from Digital. The interaction force observed between the sample and the surface was approximately 50nN [20]. The 4 samples that underwent to the different cleaning solutions based on NH_4OH were dipped in 40H_2O : 1HF for 30 s, followed by a rinse in DI water for 60 seconds to remove the native oxide. Then, these samples were analyzed by atomic force microscopy in the same way already described.

MOS capacitors were manufactured on these previously cleaned wafers with low micro-roughness and the lowest NH_4OH content of the four previously evaluated cleaning procedures.

Following, gate oxides were grown on flat and with vertical steps (trenches). The depth of the steps was set at 100 nm, which is about an order of magnitude greater than the thickness of the oxide to be grown. Figure 1 schematically illustrates the MOS capacitor on an irregular surface formed by trenches with height h = 100 nm on which gate silicon oxide was grown. The fabrication process of MOS capacitors was based on the previous analysis of the cleaning procedures using the baths 1, 2, 3 and 4 and a complete recipe for chemical cleaning will be proposed as a modification of a standard RCA cleaning for the gate pre-oxidation process, which will be presented in the Results and Discussion.

After performing the pre-oxidation cleaning recipe, lithography and plasma etching of the silicon samples were performed to define the steps. For plasma etching, SF_6 was used (flow of 25 sccm, power of 150 W and pressure of 50 mTorr for 40 seconds) and the etching time was adjusted to obtain a step height of 100 nm with the aid of the profilometry technique. The height standard deviation along 3-inch diameter wafers was approximately 5%. The masks used in the lithographic process were designed with trench widths of 30 μm. Subsequently, over the trenches, MOS capacitors with an area of 300 μm x 300 μm were defined.

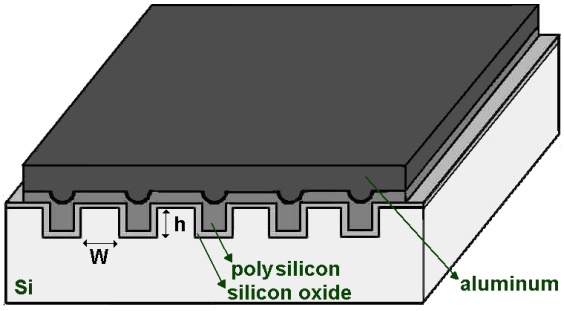


Fig. 1 - Schematic representation of the MOS capacitor with an area of 300 μm x 300 μm manufactured on an irregular surface composed of trenches with height h = 100 nm and width W = 30 μm.

Then, the slides with trenches and some reference plane slides were submitted to two distinct recipes of oxidation. The first type of oxidation was the conventional one, carried out at a temperature of 850ºC, with an ultra pure oxygen flow of 1.1 L/min. for 10 min. on flat wafers and on wafers with trenches. The second type was the pyrogenic oxidation, at a temperature of 850ºC, with an ultra pure oxygen flow of 2 L/min. and 1 L/min. of a mixture of N_2+10%H_2 for 10 min. and, in this case, flat wafers and wafers with trenches were also used. An important care was taken during the introduction of hydrogen and oxygen gases into the process furnace to avoid explosion hazards by setting the H_2/O_2 weight ratio less than 2 [21]. After oxidation, the wafers underwent to the following steps:

1- Deposition of polycrystalline silicon (500 nm) by LPCVD (Low Pressure Chemical Vapor Deposition)
2- Doping of polycrystalline silicon, using the SOG (Spin On Glass), that is, diffusion of dopant in the polycrystalline silicon from oxide doped through annealing at a temperature of 1050ºC for 20 min.;
3- Deposition of aluminum (200 nm) by thermal evaporation;
4- Photolithography and dry etching of aluminum in SF_6 followed by a wet corrosion of polycrystalline silicon to define the MOS capacitor structure;
5- Deposition of aluminum on the backside of the wafer;
6- Final sintering at 420ºC for 20min. in N_2 +10%H_2 [18].

After the fabrication of the MOS capacitors, the silicon oxides grown were electrically characterized. First, with the aid of an HP4140 equipmentm the high and low frequency CxV curves were measured and the parameters thickness of the gate oxide (X_o), concentration of dopants in the substrate P (N_B), effective density of charges in the oxide (Q_{SS}/q) and interface state density (D_{it}) were extracted [19]. Subsequently, with the aid of the HP4280 equipment, IxV measurements were performed using a voltage ramp of 0.2 V/s in order to extract the breakdown current, breakdown voltage, breakdown current density and effective breakdown field. Table I summarizes the main parameters obtained from the oxides grown on flat wafers or with trenches and, using conventional or pyrogenic processes with the respective names (letter "A" for flat surface, letters "B" and "C" for wafers with trenches, letter "p" to indicate pyrogenic oxidation and letter "o" to indicate conventional oxidation).

TABLE I
SUMMARY OF THE MAIN MANUFACTURING CHARACTERISTICS OF THE SAMPLES

Wafer	Surface type	Oxidation Process	Temperature (ºC)
Ao	Flat	conventional	850
Bo	Trench	conventional	850
Co	Trench	conventional	850
Ap	Flat	pyrogenic	850
Bp	Trench	pyrogenic	850
Cp	Trench	pyrogenic	850

III. RESULTS AND DISCUSSION

Tables II and III show the surface roughness results RMS (R_{RMS}), mean (R_a) and valley-peak ($R_{v\text{-}p\ max}$), obtained for the samples that were underwent to the different solutions SC1 at different temperatures for scanning 1µm x 1µm.

It is observed in Table II for 71ºC and, in Table III, for 84ºC, that there was a tendency of micro-roughness decrease when the volumetric concentration of NH_4OH is varied from 1 to 0.25. It was also observed the growth of a native oxide whose thickness was approximately 5nm for all the samples, according to ellipsometry measurements for a fixed index of refraction of 1.465 [5]. This thin native oxide has a substantial effect on the obtained roughness obtained as will be shown in the following.

TABLE II
SURFACE MICRO-ROUGHNESS OBTAINED BY AFM FOR BATHS WITH DIFFERENT CONCENTRATIONS OF NH_4OH AT 71ºC. NOTE THAT SAMPLE "REF" IS THE REFERENCE SAMPLE (AS RECEIVED WAFER WITHOUT TREATMENT)

1µm x 1µm AFM scanning	R_{RMS} (nm)	R_a (nm)	$R_{v\text{-}p\ max}$ (nm)
REF	0.086	0.065	1.424
$4H_2O$:$1H_2O_2$:0.25NH_4OH	0.100	0.079	0.888
$4H_2O$:$1H_2O_2$:1NH_4OH	0.127	0.093	1.985
$4H_2O$:$1H_2O_2$:2NH_4OH	0.103	0.081	1.326
$4H_2O$:$1H_2O_2$:5NH_4OH	0.125	0.099	1.139

TABLE III
SURFACE MICRO-ROUGHNESS OBTAINED BY AFM FOR BATHS WITH DIFFERENT CONCENTRATIONS OF NH_4OH AT 84ºC. NOTE THAT SAMPLE "REF" IS THE REFERENCE SAMPLE (AS RECEIVED WAFER WITHOUT TREATMENT)

1µm x 1µm AFM scanning	R_{RMS} (nm)	R_a (nm)	$R_{v\text{-}p\ max}$ (nm)
REF	0.086	0.065	1.424
$4H_2O$:$1H_2O_2$:0.25NH_4OH	0.086	0.065	1.241
$4H_2O$:$1H_2O_2$:1NH_4OH	0.137	0.104	1.536
$4H_2O$:$1H_2O_2$:2NH_4OH	0.093	0.072	1.035
$4H_2O$:$1H_2O_2$:5NH_4OH	0.099	0.078	0.980

TABLE IV
SURFACE MICRO-ROUGHNESS OBTAINED FROM AFM FOR SOLUTIONS WITH DIFFERENT CONCENTRATIONS OF NH_4OH AT 71ºC. "REF+" REPRESENTS THE REFERENCE SAMPLE THAT UNDERWENT A 30 S "DIP" IN DILLUTED HF

1µm x 1µm AFM scanning	R_{RMS} (nm)	R_a (nm)	$R_{v\text{-}p\ max}$ (nm)
REF+	0.068	0.054	0.607
$4H_2O$:$1H_2O_2$:0.25NH_4OH	0.069	0.054	0.616
$4H_2O$:$1H_2O_2$:1NH_4OH	0.068	0.054	0.601
$4H_2O$:$1H_2O_2$:2NH_4OH	0.062	0.050	0.539
$4H_2O$:$1H_2O_2$:5NH_4OH	0.072	0.057	0.834

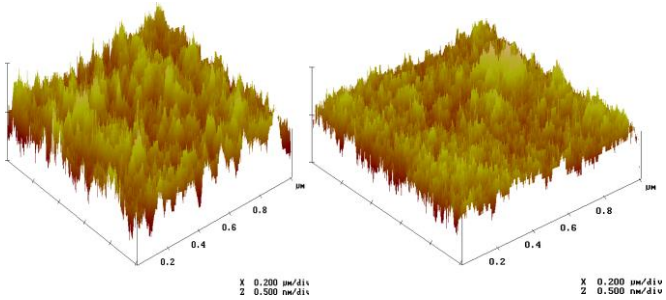
TABLE V
SURFACE MICRO-ROUGHNESS OBTAINED FROM AFM FOR SOLUTIONS WITH DIFFERENT CONCENTRATIONS OF NH_4OH AT 84ºC. "REF+" REPRESENTS THE REFERENCE SAMPLE THAT UNDERWENT A 30 S "DIP" IN DILLUTED HF

1µm x 1µm AFM scanning	R_{RMS} (nm)	R_a (nm)	$R_{v\text{-}p\ max}$ (nm)
REF+	0.068	0.054	0.607
$4H_2O$:$1H_2O_2$:0.25NH_4OH	0.075	0.058	1.164
$4H_2O$:$1H_2O_2$:1NH_4OH	0.068	0.054	0.637

$4H_2O:1H_2O_2:2NH_4OH$	0.065	0.051	0.560
$4H_2O:1H_2O_2:5NH_4OH$	0.065	0.052	0.552

The processed samples according to Tables II and III were dipped in a solution of 1HF: $40H_2O$ for 30 s at room temperature, followed by rinsing in DI water for 60 s. After this procedure, the native oxide was completely removed and AFM measurements were performed to obtain the surface roughness parameters. The results obtained are shown in Tables IV and V.

Figure 2 shows 3D images of the reference sample (as-received wafers without any treatment (REF+) and of the sample processed in $4H_2O:1H_2O_2:0.25NH_4OH$ at 71ºC during 15 min followed by dip in $1HF:40H_2O$ during 30s for a scan area of 1 µm x 1 µm. It is important to point out that the removal of the native oxide after immersion in $4H_2O:1H_2O_2:0.25NH_4OH$ at 71ºC for 15 min means low roughness parameters (R_{RMS}, R_a and $R_{v\text{-}p\ max}$) in the Table IV with the lowest content of NH_4OH.



(a) **(b)**

Fig. 2 - 3D images obtained by AFM in 1 µm x 1 µm areas for : (a) as-received wafer (no treatment), (b) sample processed in $4H_2O:1H_2O_2:0.25NH_4OH$ at 71ºC for 15 min followed by dip in $1HF:40H_2O$ during 30s.

Comparing the micro-roughness parameters presented in Tables II and III with those presented in Tables IV and V, it is possible to conclude that the dip step in diluted HF solution means a substantial decrease of the micro-roughness parameters. It can be inferred that this behavior is due to the surface characteristics of the native oxide which is grown on the surface during immersion in the baths indicated in Tables II and III. Removal of these native oxide layers lead to bare silicon surfaces with less micro-roughness as shown in Tables IV and V. After the dip step in a diluted HF solution, the surface becomes hydrophobic, as pointed out in the literature [22]. At the same time, the diluted concentration of HF used does not damage the surface of the wafers [22]. In addition, the maximum time interval of 5 min. between the end of the dip process in diluted HF solution and the AFM data acquisition of the surface topography ensures a surface practically free of native oxide[22].

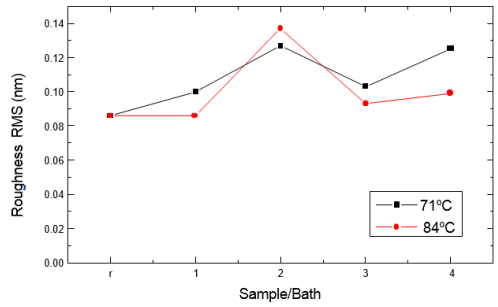


Fig. 3 - RMS roughness obtained by AFM for samples 1, 2, 3 and 4 and reference as indicated in Tables II and III.

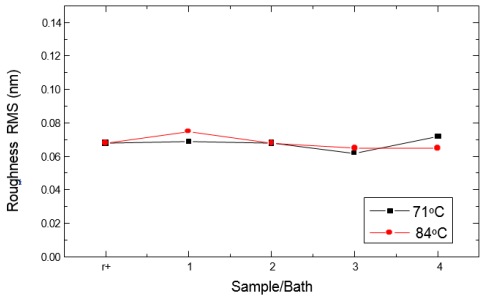


Fig. 4 - RMS roughness obtained by AFM for samples 1, 2, 3 and 4 and reference as indicated in Tables II and III.

Figure 3 shows the RMS roughness for the different samples (as-received, and the samples that underwent to the baths 1, 2, 3 and 4 indicated in Tables II, III, IV and V) and the two bath temperatures used. Figure 4 corresponds to the same samples processed after immersion in dilute HF solution. In addition to the substantial reduction in surface micro-roughness after the native oxide removal, lower micro-roughness is observed at 71ºC for samples that did not undergo the dip in HF diluted solution, possibly due to surface oxidation with a greater degree of unevenness promoted by the OH species at lower temperatures.

Based on the previous analysis of the cleaning procedures using the baths 1, 2, 3 and 4, a complete recipe for chemical cleaning will be proposed as a modification of a standard RCA cleaning for the gate pre-oxidation process, which will be presented in the following. In particular, the lowest micro-roughness parameters (R_{RMS}, R_a and $R_{v\text{-}p\ max}$) can be optimized with the addition of a low content of HNO_3 [23], for example, the $20H_2O$: 1HF : $0.25HNO_3$ dip after immersion in $4H_2O:1H_2O_2:0.25NH_4OH$ at 84ºC during 15 min, with the lowest content of NH_4OH, allows one R_{RMS} = 0.062 nm R_a = 0.038 nm and $R_{v\text{-}p\ max}$ = 0.960 nm.

For the fabrication process of MOS capacitors, initially, the silicon wafers underwent a chemical cleaning procedure to obtain the lowest micro-roughness and remove metallic contaminants and particulate matter, comprising the previous immersion in the NH_4OH-based solution followed by ummersion in $1HCl/H_2O_2/4H_2O$-based solution [5,10] and

dip in $20H_2O$: 1HF : $0.25HNO_3$, whose detailing is presented in the following:

1- Rinse in deionized water for 5 min.;
2- Immersion in $0.25NH_4OH(35\%)$: $1H_2O_2$ solution for 15 min. at a temperature of 84ºC;
3- Rinse in deionized water for 5 min.;
4- Immersion in 1HCl(36%) solution: $1H_2O_2(30\%)$: $4H_2O$ for 15 min. at a temperature of 80ºC;
5- Rinse in deionized water for 5 min.;
6- Immersion in $0.25HNO_3(65\%)$ solution: 1HF(49%): 20 H_2O for 30s. at room temperature.

After the fabrication of the MOS capacitors, they were electrically characterized. Figure 4 illustrates the typical capacitance x voltage (CV) curves of high (1MHz) and low frequency (100kHz) typical for a capacitor with an area of 300 µm x 300 µm where it is possible to observe a stretching of the curves at the depletion region due to interface states. Additionally, there is a "peak" in the transition from the depletion to the inversion regions in the low frequency curve, which is associated to interface states concentration greater than $1x10^{11}$ $eV^{-1}cm^{-2}$ [19].

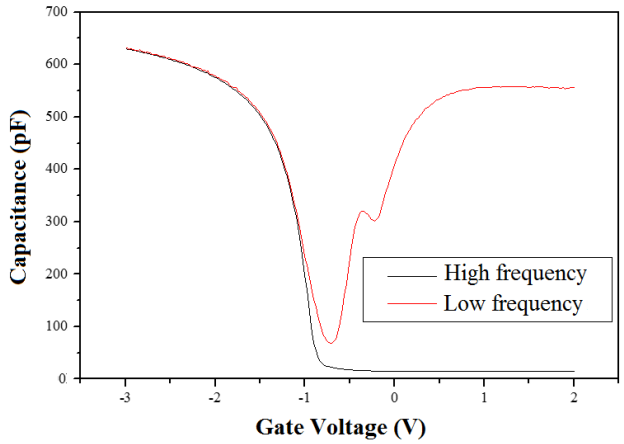


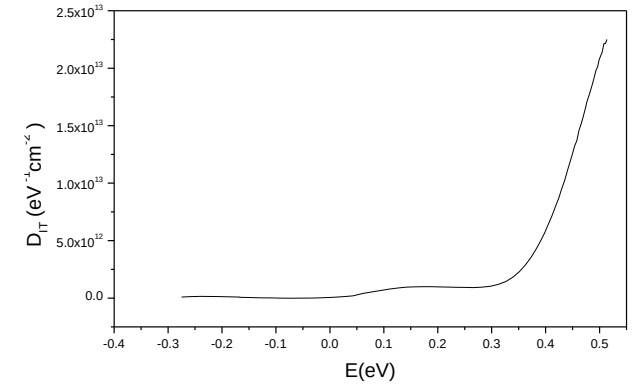
Fig. 5 - Typical high (1MHz) and low frequency (100kHz) capacitance x voltage curves for a capacitor with an area of 300 µm x 300 µm on flat wafers that have undergone conventional oxidation.

Table VI shows the values of oxide thickness (X_o), dopants concentration (N_B), effective charge density in the oxide (Q_{SS}/q) and density of interface states (D_{it}) extracted from the high and low frequency CxV [19]. These parameters refer to samples processed as summarized in Table I, that is, capacitors with and without trenches, 100 nm in height and for gate oxides obtained by conventional or pyrogenic process.

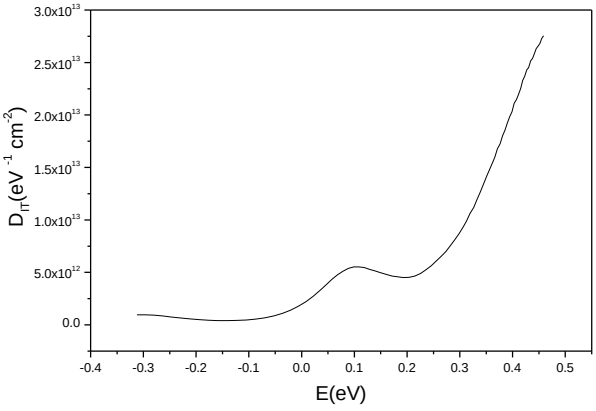
TABLE VI
PARAMETERS EXTRACTED FROM THE HIGH AND LOW FREQUENCY CXV CURVES: OXIDE THICKNESS (X_o), DOPANTS CONCENTRATION (N_B), EFFECTIVE CHARGE DENSITY (Q_{SS}/Q) AND INTERFACE STATE DENSITY (D_{IT})

Wafer	X_o (nm)	N_B ($10^{15}cm^{-3}$)	Q_{SS}/q ($10^{11}cm^{-2}$)	D_{it} (10^{11} ev^{-1} cm^{-2})
Ap	5.6±0.4	1.4±0.2	3.6±0.1	1.5±0.3
Bp	3.9±0.1	2.1±0.7	3.3±0.6	17.1±3.0
Cp	4.9±0.1	2.0±0.1	3.3±0.1	12.3±5.0
Ao	4.2±0.1	3.4±0.3	4.2±0.1	2.7±0.3
Bo	4.3±0.1	3.3±1.1	3.8±0.1	9.5±4.0
Co	4.3±0.1	2.1±0.6	3.3±0.5	11.2±3.0

It is important to highlight that the samples Ap, Bp and Cp using pyrogenic process showed a maximum thickness deviation of 7.0% for each wafer individually, while the deviation from wafer to wafer reached 43.6% which is considerably high compared to MOS manufacturing technologies whose deviations are usually controlled below 1.5% [18]. On the other hand, Ao, Bo and Co samples, whose gate oxides were obtained by conventional process, showed a maximum thickness dispersion equal to 2.5% for each individual wafer, while the maximum dispersion from wafer to wafer also reached a maximum 2.5%. All deviations shown in Table VI were obtained from 25 measurements performed on each wafer.



(a)



(b)

Fig. 6 - Typical curves of interface states density (Dit) as a function of energy (E) along the forbidden band with reference to the middle of the band (0eV) for: (a) Sample A (flat wafer) processed according to the pyrogenic recipe and (b) Sample B (wafer with trenches) also processed according to the pyrogenic recipe.

Based on the deviations shown in Table VI, it is concluded

that the pyrogenic oxidation process has greater unevenness in thickness. This fact can be associated with a higher rate of oxidation by water molecules in (3) generated from (2) during the pyrogenic process and which possibly proceeded in a non-homogeneous way along each wafer. This situation is associated with the direct way in which hydrogen diluted in nitrogen was introduced into the open-tube furnace. This process can be improved by increasing the number of wafers on the quartz carrier inside the furnace in order to discard those located on the edges; by increasing the partial pressure of hydrogen inside the furnace or by inserting a lead tube for a diluted hydrogen mixture to the region of the furnace where the pyrogenic oxidation is taking place. Despite this, the non-uniformity along each wafer, it was not so great when compared to the wafer-to-wafer reproducibility, and it is still possible to analyze the electrical performance from the point of view of breakdown of dielectric strength and leakage current. Also, it is important to highlight that the oxides obtained by the conventional process were comparatively more uniform and reproducible with percentage deviations slightly higher than the best ones already reported in the literature [18].

The dopant concentration in the substrate (Table IV) was in the range of $1x10^{15}$ to $4x10^{15}$ cm^{-3} compatible with resistivity (ρ) in the range of 1 to 10 Ω.cm for the batch of wafers used in our experiments with thickness (t) of 380 µm and mobility (μ) of 1000 cm^2/vs ($\rho = 1/(q\mu N_B)$).

According to the procedure described in [19], for all processed wafers, flat band voltages (V_{FB}) were obtained in the range of –0.91 to –0.94 V, the effective concentration of charges in the oxide (Q_{SS}/q) in the range of $3.0x10^{11}$ to $4x10^{11}$ cm^{-2}, for both pyrogenic and conventional processes, regardless of whether flat surfaces were used or not. The literature reports values about one order of magnitude smaller in the best case, that is, effective charge concentration around of $1x10^{10}$ cm^{-2} and prohibitively high values in the range $5x10^{12}$ cm^{-2} [18,19]. Therefore, the values obtained in this work can be considered reasonable and can still be optimized by increasing the thermal budget in a N_2+10%H_2 (green gas) not only to improve the interface quality regarding incomplete bonds (dangling bonds), but also to decrease the concentration of fixed charges at the Si/SiO_2 interface [18,19].

Table VI also shows the density of interface states in the middle of the forbidden band ($E=E_i$). A clear difference of about one order of magnitude can be observed between flat samples and samples with a trench, regardless of having undergone a pyrogenic or conventional process. Figure 6 shows typical curves of interface states density (D_{it}) as a function of energy along the forbidden band, having as reference the middle of the forbidden band, for which was set E_i = 0 eV as reference. It is important to highlight that the distributions presented in Figure 6 do not have the "U" shape characteristic of Si-Polycrystalline/SiO_2/Si structures as reported in the literature [19], that is, the D_{it} distribution only increases to positive energies close to the E_C conduction level ($E \approx 0.55$ eV) and not, for negative values. The fact that the distribution does not have the "U" shape is associated with the predominance of interface states along the forbidden range with acceptor character [24]. Therefore, the states charge are negative as the energy band diagram curves towards inversion. Taking N_{it} as any state in the middle of the forbidden band at the SiO_2/Si interface, its acceptor character can be given by:

$$N_{it} + e \rightarrow N_{it}^{-} \quad (4)$$

where the states occupied by electrons comprise the range from E_V to E_F along the SiO_2/Si interface and the states not occupied by electrons comprise the range from E_F to E_C [19].

The peak that appears in the D_{it} distribution shown in Figure 6(b) and does not appear in Figure 6(a) is an effect observed only for trench capacitors and that causes the D_{it} value to rise close to the middle of the forbidden band. as reported in Table VI (E = 0). This peak is associated with a non-planar surface containing steep steps at the edges of the trenches and can be understood as follows: D_{it} is higher due to the edge effect and will not correspond to the bending of the energy band as in the case of a flat surface since there is a local enhancement of the electric field along these edges. Therefore, the value of D_{it} obtained in this way is apparent and corresponds to a particular measurement situation in which charged states respond with a higher capacitance (C_{it}).

Figure 7 shows a typical I x V curve obtained for a MOS capacitor manufactured on a surface with trenches and gate oxide grown by the conventional process. The breakdown voltage and breakdown current are indicated at the breaking point of the dielectric strength and the saturation at 0.01 A corresponds to the maximum current limitation of the measuring equipment used.

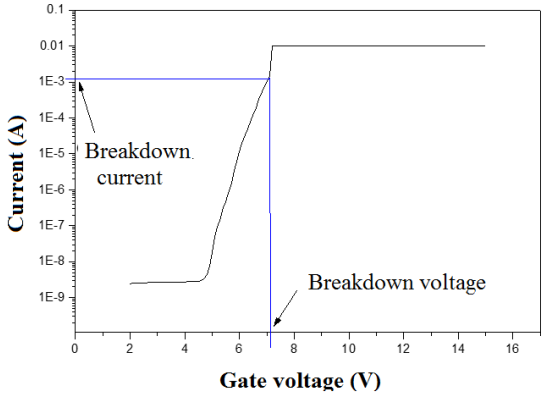


Fig. 7 - Typical I x V curve obtained for a MOS capacitor built on a surface with trenches and gate oxide grown by the conventional process.

Table VII shows the mean values and standard deviations of the breakdown current (I_{bd}), breakdown voltage (V_{bd}), thickness of the gate oxide obtained from of the CV curve (X_o), breakdown current density (J_{bd}), breakdown electric field ($E_{bd} = (V_{bd} + \phi_{MS})/X_o$) and fabrication yield (FY: percentage of capacitors that breaks down above 3 MV /cm). All the parameters were extracted in the accumulation region.

The breakdown current density (J_{bd}) and breakdown electric field (E_{bd}) were obtained from breakdown current and breakdown voltage, respectively. The J_{bd} and E_{bd} are average

values for the capacitors that did not show early failures (E_{bd} < 3 MV/cm). Two features were observed for all oxides: early failure or failures close to the intrinsic value (E_{bd} > 10 MV/cm) and failures for medium fields were not observed. In this case, the FY parameter in Table VII is the percentage of capacitors that failed above 10 MV/cm. Thus, the highest fabrication yields were observed for flat surfaces, with a substantial decrease in this parameter for wafers with trenches processed according to the pyrogenic recipe (44% and 54% for two identically processed wafers) while the fabrication yield was higher for trench wafers processed according to the conventional recipe (59% and 62% for two identically processed wafers). The decrease in fabrication yield is due to the increase of the electric field at the edges and corners of the trenches, which must be promoting early breakage of the dielectric strength. Therefore, the FY parameter can also be considered an indirect average index of the degree of coverage over steps for the trenched wafers.

TABLE VII
AVERAGE VALUES OF BREAKING CURRENT (I_{BD}), BREAKING VOLTAGE (V_{BD}), GATE OXIDE THICKNESS (X_O), BREAKING CURRENT DENSITY (J_{BD}), BREAKING FIELD (E_{BD}) AND FABRICATION YIELD (FY) FOR A SET OF 30 CAPACITORS PER WAFER.

Wafer	I_{bd} (mA)	V_{bd} (V)	X_o (nm)	J_{bd} (A/cm^2)	E_{bd} (MV/cm)	FY (%)
Ap	6.5±3.9	7.2±0.1	5.6±0.4	7.2±4.3	11.3±0.3	78
Bp	2.4±3.7	6.3±0.4	3.9±0.1	2.7±4.1	14.1±1.2	44
Cp	8.1±3.3	6.6±0.6	4.9±0.1	9.0±3.7	11.8±2.1	54
Ao	4.1±3.0	7.2±0.4	4.2±0.1	8.0±3.3	15.2±1.6	96
Bo	0.55±0.82	6.5±0.7	4.3±0.1	0.61±0.80	13.1±2.3	59
Co	0.23±0.15	6.4±0.3	4.3±0.1	0.26±0.17	11.9±0.7	62

It is also important to highlight the behavior of the maximum current density at the point where the breakdown occurs. It is observed that the wafers processed according to the pyrogenic recipe, despite having the lowest manufacturing yield, support higher current densities immediately after the breakdown event, even with values of the same order of magnitude as those obtained for flat wafers. On the other hand, the wafers with trenches processed according to the conventional recipe, presented current density one order of magnitude lower immediately before the breakdown event. This fact must be linked to the better structural quality of pyrogenic oxides compared to conventional ones where the damage process due to high current must be delayed in the pyrogenic case because the oxide not only must have better quality at the edges and corner, possibly due to smoothing and surface tension compensation associated with the presence of hydrogen in the oxidation process [18].

IV. CONCLUSION

Thin films of silicon oxide were grown on surfaces of silicon wafers containing periodic rectangular shapes with 100 nm in height. Silicon oxides (SiO_2) about 4.5 nm thick were grown in ultrapure oxygen (O_2) or pyrogenic (O_2 + H_2) environments. It was shown that pyrogenic or conventional oxidation at a temperature of 850ºC allows obtaining gate oxides on steps with a high breakdown field (>10 MV/cm), good planar uniformity and good coverage at the edges of the steps.

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